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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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10/520,691

07/26/2005

Xinming Shi

9896-057/NP

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27572 7590 02/13/2008
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EXAMINER

THOMPSON, JR, OTIS L

ART UNIT

PAPER NUMBER

4183

MAIL DATE

DELIVERY MODE

02/13/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

| | | | |
|------------------------------|---|-------------------------------------|--|
| Office Action Summary | Application No. 10/520,691 | Applicant(s) SHI, XINMING | |
| | Examiner OTIS L. THOMPSON, JR | Art Unit 4183 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 January 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☐ Claim(s) _____ is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>05/14/2007 10/02/2007 04/26/2005</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art Olson (US 6,438,625 B1) in view of admitted prior art Gleeson et al. (US 6,763,023).

3. Regarding claim 1 setting step, Olson discloses that primary address pins in the primary backplane (**centralized exchanging and controlling unit**) slots are coupled so as to set the primary address pins in each primary backplane slot to a unique value (Abstract).

Regarding claim 1 connecting step, Olson discloses a computer controlled system has two or more secondary backplanes (**module**) that are plugged into slots (**communication control interface module**) in a primary backplane (Abstract).

Regarding claim 3, Olson discloses that board slots in the secondary backplanes are assigned unique addresses, and the range of addresses for each secondary backplane is contiguous with the range of addresses for a neighboring secondary backplane (Abstract). Olson further discloses that each slot has a unique binary identification or address that may be used to identify communications between the board in a particular slot and control devices such as a host computer. Each slot has a

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number of address pins and each board has a corresponding number of board pins. Each address pin of the slot and the corresponding board pin on the board are used to communicate one bit of the slot address (Column 1, lines 25-36).

Regarding claim 4, Olson discloses that each of the board slot address pins is coupled to a respective one of the bus lines so as to set that address pin to a value that is determined by the voltage on that bus line (Column 2, lines 48-51).

Olson does not specifically disclose the **communicating step of claim 1** and **sending step of claim 5** wherein a communication message is sent to the centralized exchanging and controlling unit by a source module, processed by the centralized exchanging and controlling unit, and forwarded to a destination module by the centralized exchanging and controlling unit. Olson also does not specifically disclose the **broadcasting step of claim 2** wherein a destination address of a message is compared with address of each module in the centralized exchanging and controlling unit, and when an address is found, the message is forwarded to the module.

However, Gleeson et al. discloses, **regarding claims 1 and 5**, a network switch that performs the aforementioned method. Figure 3 illustrates this process. In step 31, a packet is received at a network switch (**centralized exchange and controlling unit**) from a source address (or source device). In step 34, the destination address is determined by the network switch, and the packet is forwarded to its destination in step 35.

Gleeson et al. further discloses, **regarding claim 2**, the flooding or broadcasting of a packet at step 36 of the process shown in figure 3. This means that a copy of the packet (**message**) is supplied to all (or all of a selected plurality) of the ports (**modules**) in order to determine the destination network address (Column 4, lines 23-40). Once the

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address is found, the packet (**message**) is sent to and received by the module connected to the corresponding port.

The benefit of the process in figure 3 of Gleeson et al., as it pertains to applicant's claims 1,2, and 5, is that it incorporates a learning process for MAC (physical) addresses that are typical to a particular network switch (**centralized exchange and controlling unit**) (Column 3, lines 66-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to incorporate the teachings of Gleeson et al. into Olson in order to learn physical addresses that are typical to a particular network switch (**centralized exchange and controlling unit**).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Jennings et al. (US 6,807,175 B1) discloses distributed multicast routing in packet-based communication network devices. Engbersen et al. (US 2002/0080775 A1) discloses switching nodes and interface modules for data networks. Kusyik et al. (US 6,510,056 B1) discloses a hinged removable connector module.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to OTIS L. THOMPSON, JR whose telephone number is (571)270-1953. The examiner can normally be reached on Monday to Thursday 7:30 am to 5:00 pm EST.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Len Tran can be reached on (571)272-1184. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Otis L Thompson, Jr./
Examiner, Art Unit 4183
January 7, 2008

/Len Tran/
Supervisory Patent Examiner, Art Unit 4183